TIRUYE MULAT AYINET

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PROFESSIONAL SUMMARY

PhD researcher at DISI, University of Trento, with an M.Sc. in Computer Engineering, specializing in intelligent and programmable networked systems, 5G/6G wireless architectures, and machine learning for resource-constrained networked systems. Published in IEEE venues with demonstrated ability to work across AI model development, hardware acceleration, and system-level performance evaluation. Hands-on background in building end-to-end SRv6-based service chaining frameworks, cloud-native CNF/VNF orchestration, and AI-guided optimization pipelines. Motivated to contribute to next-generation intelligent computing infrastructures through research at the intersection of machine learning, cloud-native systems, and AI-driven network optimization.

RESEARCH INTERESTS

- **AI-Native Programmable Networks:** SDN/NFV, SRv6-based service function chaining, VNF/CNF placement, network slicing, and deployment-aware orchestration.
- **5G/6G Wireless & Non-Terrestrial Networks:** AI-driven O-RAN, RIS-assisted communications, and integrated terrestrial/NTN architectures with QoS and energy-efficiency focus.
- **Edge-Native ML & Resource-Aware Scheduling:** Federated learning, TinyML, continual learning, and energy-performance optimization for edge-cloud and embedded environments.
- **Autonomous Security for Networked Systems:** ML-based intrusion detection, zero-touch security orchestration, and policy enforcement for SDN/NFV-enabled 5G/6G infrastructures.

EDUCATION

Ph.D. in Information Engineering and Computer Science

DISI, University of Trento, Italy 2026 – Present

M.Sc. in Computer Engineering

University of Pisa, Italy Sep 2023 – Feb 2026

Thesis: Implementation and Integration of SRv6-based NFV Chaining and Energy-Aware Optimization in the OMNeT++/INET Simulation Framework

Supervisors: Prof. Antonio Virdis, Prof. Enzo Mingozzi, Dr. Federico Casu

Dual Masters in Nano Electronic Engineering and Design

Singapore University of Technology and Design (SUTD) & Chang Gung University (CGU), Singapore/Taiwan Sep 2021 – Mar 2023

Thesis: Dual Mode Systolic Array-based Processing Element for CNN Accelerator

Supervisors: TEO, Tee Hui; Co-advisors: WEY, I-Chyn and CHOW, Hwang Cherng

B.Tech. in Electronics and Electrical Engineering

Kalinga Institute of Industrial Technology (KIIT) University, India Jul 2017 – Aug 2021

Thesis: Direction of Arrival (DOA) Estimation using ESPRIT Algorithm

Supervisor: Prof. Sambit Prasad Kar

PUBLICATIONS

Peer-Reviewed (IEEE)

1. **M. A. Tiruye**, T. A. Muche, and T. A. Tesfamichael, "AI-Optimized Federated Learning with Dynamic Scheduling for High-Performance Computing," 2025 IEEE 4th International Conference on Computing and Machine Intelligence (ICMI), Mount Pleasant, MI, USA, 05–06 April 2025. DOI: 10.1109/ICMI65310.2025.11141301.
2. **M. A. Tiruye**, O. B. Gerba, and T. H. Teo, "A 155 MHz Low-Jitter PLL for Enhanced Signal Integrity in High-Speed Interconnects," 2024 IEEE 33rd Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), Toronto, ON, Canada, pp. 1–3, 06–09 October 2024. DOI: 10.1109/EPEPS61853.2024.10754287. ISSN: 2165-4115.

3. S. H. Chua, T. H. Teo, **M. A. Tiruye**, and I.-C. Wey, "Systolic Array Based Convolutional Neural Network Inference on FPGA," 2022 IEEE 15th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Penang, Malaysia, pp. 128–133, 19–22 December 2022. DOI: 10.1109/MCSoC57363.2022.00029. ISSN: 2771-3075.
4. T. R. Loo, T. H. Teo, **M. A. Tiruye**, and I.-C. Wey, "High-Performance Asynchronous CNN Accelerator with Early Termination," 2022 IEEE 15th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Penang, Malaysia, pp. 140–144, 19–22 December 2022. DOI: 10.1109/MCSoC57363.2022.00031. ISSN: 2771-3075.

RESEARCH EXPERIENCE

MSc Research — Programmable Networked Systems | University of Pisa | Jul 2025 – Feb 2026

- Built an end-to-end SRv6-based Service Function Chaining (SFC) simulation framework by extending OMNeT++/INET, enabling research on next-generation programmable network architectures.
- Developed data and control planes implementing packet-level IPv6 traffic steering, integrating an energy/resource-aware NFVO optimization module for VNF/CNF placement under strict deployment constraints.
- Engineered a repeatable orchestration workflow for evaluating multi-function service chains (firewalls, IDS) across diverse topologies, unifying steering policy enforcement, observability, and resilient chaining.

MSc Research — Hardware-Efficient CNN Accelerator Design | SUTD/CGU | Jun 2022 – Mar 2023

- Designed a Dual-Mode Systolic Array-based Processing Element for CNN acceleration, supporting convolution and fully-connected layers in a unified architecture for flexible high-throughput inference on constrained silicon.
- Optimized dataflow scheduling and PE array utilization targeting area-performance tradeoffs critical for embedded and edge AI deployment.
- Co-authored two peer-reviewed IEEE publications at MCSoC 2022 on FPGA-based CNN inference and asynchronous CNN acceleration with early termination.

SELECTED PROJECTS

ARISE-6G: AI-Assisted Cloud-Native O-RAN & Hybrid RIS Orchestration | Jan 2026 – Present

- Developed a software-defined 5G/6G orchestration framework integrating SMO, Non-RT/Near-RT RIC, O-RAN split control, cloud-native CNF/VNF placement, and hybrid RIS-assisted optimization.
- Built an end-to-end QoS-aware multi-user control pipeline with AI-guided optimization using DRL, factorized policies, and deep-unfolding approaches.
- Extending toward NTN access awareness, SDR waveform adaptation, and service steering under latency, energy, and resilience constraints.

NOVA-6G: AI-Driven Orchestration for 5G/6G Networks: A Digital Twin Approach | Sep 2025 – Jan 2026

- Built a Digital Twin for autonomous 5G/6G network management integrating a PPO reinforcement learning agent within a custom Gymnasium environment, achieving multi-objective optimization across carbon intensity, energy cost, SLA compliance, and resilience simultaneously
- Implemented a closed-loop autonomous event agent (ETSI ZSM / ETSI NFV IFA 007) with automated HEAL/MIGRATE/SCALE/TERMINATE lifecycle operations achieving < 50ms MTTR, with Gemini LLM-generated NIS2/DORA-compliant incident reports
- Designed an Intent-Based Networking engine (IETF RFC 9315) enabling natural language network policy enforcement with continuous closed-loop validation against live telemetry and carbon-aware VNF placement per EU Green Deal targets
- Architected an N+1 Active/Standby resilience framework targeting 6G URLLC five-nines (99.999%) availability with sub-50ms failover; designed for O-RAN Near-RT RIC deployment as an xApp via E2/A1 interfaces with Open5GS + UeRansim testbed

Network Automation System | Dec 2024 – Feb 2025

- Automated the provisioning of arista switch router configurations by creating scripts that generated device configs using predefined IP addressing, AS numbers, and BGP neighbors.
- Reduced manual configuration time by 80% and minimized human error using Python based templating

TinyOrchestra — Federated TinyML for Networked Embedded Systems | Nov 2024 – Jan 2025

- Designed a decentralized intelligence framework enabling on-device inference and local adaptation on nodes with as little as 256KB RAM, using Post-Training Quantization (FP32 to Int8) for 75% memory reduction.
- Implemented Federated Averaging (FedAvg) across a 12-node simulated mesh, transmitting only model weight deltas, achieving 92% bandwidth reduction over raw data streaming.

NeuroStream — Neuromorphic Continual Learning for Sustainable Edge AI | Sep 2024 – Dec 2024

- Implemented a Spiking Neural Network using Leaky Integrate-and-Fire neurons with 25-timestep temporal processing, achieving significant energy efficiency gains over conventional ANN architectures.
- Applied Elastic Weight Consolidation (EWC) via Fisher Information Matrix to prevent catastrophic forgetting in continual learning, retaining 95%+ prior task performance across sequential tasks.

SKILLS

- **Programming Languages:** Python, C++, C, Java, Bash
- **Networking & Systems:** IPv4/IPv6, P4, SRv6, OSPF/BGP, Segment Routing/MPLS, NFV, SDN, SDR
- **Testbeds & Simulators:** Open5GS, UERANSIM/srsRAN, O-RAN, OMNeT++/INET, MATLAB
- **ML/DL Frameworks:** PyTorch, TensorFlow, TFF, snnTorch, Scikit-learn, Keras
- **Messaging & Data Exchange**: Kafka, RabbitMQ, gRPC, REST APIs, Protocol Buffers
- **Databases**: PostgreSQL, MongoDB, InfluxDB, Redis
- **Cloud & DevOps:** Docker, Kubernetes, OpenStack, AWS/GCP/Azure, Git, CI/CD (GitLab CI)

ACADEMIC & TEACHING EXPERIENCE

Teaching Assistant | Singapore University of Technology and Design | Jun 2022 – Mar 2023

- Supported AI-focused labs and student projects in hardware design and machine learning courses; mentored students through hands-on project development and guided independent research activities.

AWARDS & SCHOLARSHIPS

- MAECI Scholarship — Italian Government (Aug 2023 – Sep 2025)
- NEED Scholarship — Singapore University of Technology and Design (Aug 2021 – Mar 2023)
- Betere Science Scholarship — Ethiopian Government (Sep 2017 – Oct 2021)

LANGUAGES

- Amharic (Native) | English: Advanced C1 | Italian: Intermediate B1

PRIVACY STATEMENT

- I authorize the processing of my personal data in accordance with Legislative Decree 196/2003 and the GDPR (EU Regulation 2016/679) for the purposes of recruitment and personnel selection (Autorizzo il trattamento dei miei dati personali ai sensi del D. Lgs. 196/2003 e del GDPR (Regolamento UE 2016/679) ai fini della ricerca e selezione del personale).